

Description

LOW-VOLTAGE DIFFERENTIAL AMPLIFIER

BACKGROUND OF INVENTION

[0001] Technical Field

[0002] The present invention relates to electronic circuits in general, and, in particular, to differential amplifier circuits. Still more particularly, the present invention relates to a low-voltage differential amplifier circuit having a wide common mode range.

[0003] Description of Related Art

[0004] A conventional differential amplifier circuit typically includes a pair of field effect transistors with the gates as differential inputs and the drains as outputs. The conventional differential amplifier circuit also includes a current source connected to the sources of the field effect transistors to supply a fixed current to the field effect transistors. During operation, the differential voltage inputs supplied to the gates are compared, and the conductivity of one of the field effect transistors is raised whilst the con-

ductivity of the other transistor is lowered.

[0005] Conventional differential amplifier circuits are best operated in a common mode range (CMR) centered around $V_{dd}/2$. When outside the above-mentioned CMR, the outputs of conventional differential amplifier circuits may not be acceptable. Such limitation in the CMR tend to restrict the type of applications conventional differential amplifier circuits can be employed.

[0006] There are several solutions for increasing the CMR of a conventional differential amplifier circuit. However, none of the solutions allow proper operations from 0.1 to $(V_{dd} - 0.2)$ volt over the entire process, voltage and temperature (PVT) operating range. Consequently, it would be desirable to provide an improved differential amplifier circuit having a relatively wide common mode range.

SUMMARY OF INVENTION

[0007] In accordance with a preferred embodiment of the present invention, a differential amplifier circuit includes a first differential amplifier, a second differential amplifier and a summing circuit. The first differential amplifier receives a pair of differential input signals to generate a first output. The second differential amplifier receives the same pair of differential input signals to generate a second output. The

summing circuit sums the first output of the first differential amplifier and the second output of the second differential amplifier to provide a common output for the differential amplifier circuit.

[0008] All objects, features, and advantages of the present invention will become apparent in the following detailed written description.

BRIEF DESCRIPTION OF DRAWINGS

[0009] The invention itself, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0010] Figure 1 is a circuit diagram of a differential amplifier circuit, in accordance with a preferred embodiment of the present invention;

[0011] Figure 2 is a circuit diagram of a reference voltage generation circuit to be used with a summing circuit within the differential amplifier circuit from Figure 1, in accordance with a preferred embodiment of the present invention; and

[0012] Figure 3 graphically compares the common mode range of the differential amplifier circuit from Figure 1 with the

common mode range of a conventional differential amplifier circuit.

DETAILED DESCRIPTION

[0013] Referring now to the drawings and in particular to Figure 1, there is depicted a circuit diagram of a differential amplifier circuit, in accordance with a preferred embodiment of the present invention. As shown, a differential amplifier circuit 10 includes a first differential amplifier 11, a second differential amplifier 21 and a summing circuit 31. First differential amplifier 11 and second differential amplifier 21 are connected in parallel with each other and both share the respective differential inputs. The outputs of first differential amplifier 11 and second differential amplifier 21 are combined by summing circuit 31 to produce a single common output for differential amplifier circuit 10.

[0014] First differential amplifier 11 includes p-channel transistors 12–14 and n-channel transistors 15–17. P-channel transistor 13 is connected in series with n-channel transistor 15. Similarly, p-channel transistor 14 is connected in series with n-channel transistor 16. The gate and drain of p-channel transistor 13 are connected to the gate of p-channel transistor 14. P-channel transistor 12 is con-

nected between V_{dd} and the drains of p-channel transistors 13–14. N-channel transistor 17 is connected between the sources of n-channel transistors 15–16 and ground. The gate of n-channel transistor 17 is connected to V_{CMN} – a gate control voltage to control the current through n-channel transistor 17 in a consistent and predictable manner using a current mirror technique. The gate of p-channel transistor 12 is connected to an active low EN-ABLE_N signal. Because n-channel differential amplifiers 15–16 receive differential input pair-input+ and input-, first differential amplifier 11 is considered as an n-channel differential amplifier.

[0015] Second differential amplifier 21 includes p-channel transistors 22, 25–27 and n-channel transistors 23–24. P-channel transistor 25 is connected in series with n-channel transistor 23. Similarly, p-channel transistor 26 is connected in series with n-channel transistor 24. The gate and drain of n-channel transistor 23 are connected to the gate of n-channel transistor 24. P-channel transistors 22 and 27 are connected in series between V_{dd} and the sources of p-channel transistors 25–26. The gate of n-channel transistor 27 is connected to V_{CMP} – a gate control voltage to control the current through p-channel transis-

tor 27 in a consistent and predictable manner using a current mirror technique. The sources of n-channel transistors 23–24 are connected to ground. The gate of p-channel transistor 22 is connected to ENABLE_N signal. Because p-channel differential amplifiers 25–26 receive differential input pair—input+ and input–, second differential amplifier 21 is considered as a p-channel differential amplifier.

[0016] Summing circuit 31 includes p-channel transistors 32–34 and n-channel transistors 35–38. P-channel transistor 33 is connected in series with n-channel transistor 35. Similarly, p-channel transistor 34 is connected in series with n-channel transistor 36. The gate and drain of p-channel transistor 33 are connected to the gate of p-channel transistor 34. N-channel transistors 37–38 are connected in series between the sources of n-channel transistors 35–36 and ground. The gate of n-channel transistor 37 is connected V_{CMN} . The gate of n-channel transistor 35 is connected to a reference voltage V_{ref} . Reference voltage V_{ref} provides proper voltage biasing for summing circuit 31. Reference voltage V_{ref} is preferably generated by a reference voltage generation circuit shown in Figure 2. The gate of n-channel transistor 36 is connected to the output

of first differential amplifier 11 (i.e., the node between p-channel transistor 14 and n-channel transistor 16) and to the output of second differential amplifier 21 (i.e., the node between p-channel transistor 26 and n-channel transistor 24). The drain of p-channel transistor 32 is connected to the node between p-channel transistor 34 and n-channel transistor 36 to provide a single common output 39 for differential amplifier circuit 10. The gates of p-channel transistor 32 and n-channel transistor 38 are connected to an active low ENABLE_P signal. P-channel transistor 32 is a clamp device to hold output 39 high when ENABLE_P is low (i.e., inactive).

[0017] During operation, an active low ENABLE_N signal is applied to the gates of p-channel transistors 12 and 22, and an active high ENABLE_P signal is applied to p-channel transistor 32 and n-channel transistor 38. A pair of differential input signals are applied to the gates of n-channel transistor 15 and p-channel transistor 25 via input+, and to the gates of n-channel transistor 16 and p-channel transistor 26 via inputB, respectively. The output for first differential amplifier 11 is generated at the node located between p-channel transistor 14 and n-channel transistor 16. Concurrently, the output for second differential am-

plifier 21 is generated at the node located between p-channel transistor 26 and n-channel transistor 24. The outputs from first differential amplifier 11 and second differential amplifier 21, which are analog in nature, are subsequently combined by summing circuit 31 at the gate of n-channel transistor 36. In turn, summing circuit 31 provides a common output signal at output 39 for differential amplifier circuit 10.

[0018] With reference now to Figure 2, there is depicted a circuit diagram of a reference voltage generation circuit for summing circuit 31, in accordance with a preferred embodiment of the present invention. As shown, a reference voltage generation circuit 20 includes p-channel transistors 41–44 and n-channel transistors 45–46. P-channel transistors 41–42 are connected in series between V_{dd} and the sources of p-channel transistors 43–44. The gate of p-channel transistor 41 is connected to active low ENABLE_P signal. The gate of p-channel transistor 42 is connected to V_{CMP} . P-channel transistor 43 is connected in series with n-channel transistor 45. Similarly, p-channel transistor 44 is connected in series with n-channel transistor 46. The gate and drain of n-channel transistor 45 are connected to the gate of n-channel transistor 46. The sources

of n-channel transistors 45–46 are connected to ground. The gate and drain of p-channel transistor 44 are connected to the gate of p-channel transistor 43 to generate a reference voltage V_{ref} for summing circuit 31 (from Figure 1).

[0019] Referring now to Figure 3, there is illustrated a graphical comparison between the common mode range of differential amplifier circuit 10 (from Figure 1) and the common mode range of a conventional differential amplifier circuit. As shown, a pair of differential ± 50 mV input signals 51 is sent to both a conventional differential amplifier circuit and differential amplifier circuit 10, ramping from 0.0 V to approximately 0.8 V. The common mode range of the conventional differential amplifier circuit, as indicated by an output waveform 52, is not acceptable within the input voltage range of 0.1 V to 0.4 V. In contrast, the common mode range of differential amplifier circuit 10, as indicated by an output waveform 53, remains consistent throughout the input voltage range of approximately 50 mV through 0.8 V.

[0020] As has been described, the present invention provides a low-voltage differential amplifier circuit having a relatively wide common mode range. The differential amplifier cir-

cuit of the present invention allows a switch point reference to be established by shorting two differential inputs to a single output, causing the entire differential amplifier to hang-up at the unity gain switch point. The output is then utilized as the reference voltage V_{ref} input of the summing circuit to provide a nearly perfect centered reference point that tracks well over the entire voltage, process, temperature and common mode operating range.

[0021] While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.